near5 (module banks)))	08/24 11:05 07/23 11:56 07/23 11:56 07/23 11:58 07/23 12:08 07/23 09:54
- 1013 711/169 EPO; JPO USPAT; US-PGPUB; EPO	07/23 11:56 07/23 11:58 07/23 11:58
- 1013 711/169 USPAT; US-PGPUB; EPO; JPO USPAT;	07/23 11:56 07/23 11:58 07/23 11:58
US-PGPUB; EPO; JPO USPAT;	07/23 11:56 07/23 11:58 07/23 11:58
- 2376 365/194 EPO; JPO USPAT; US-PGPUB; EPO	07/23 11:58 07/23 11:58 07/23 12:08
- 2376 365/194 EPO; JPO USPAT; US-PGPUB; EPO	07/23 11:58 07/23 11:58 07/23 12:08
- 2376 365/194 USPAT; US-PGPUB; EPO; IPO USP	07/23 11:58 07/23 11:58 07/23 12:08
- 1405 (minimiz\$3 reduc\$3) near10 (delay near5 (access read write)) - 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; US-PGPUB; EPO; JPO USPAT; (access read write))) - 44 (equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; ((read write access) near6 latency) - 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; ((read write access) near6 latency) - 172 minimum near8 (device memory) near9 latency - 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO	07/23 11:58 07/23 11:58 07/23 12:08
- 1405 (minimiz\$3 reduc\$3) near10 (delay near5 (access read write)) - 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; US-PGPUB; EPO; JPO USPAT; (access read write))) - 44 (equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO USPAT; ((read write access) near6 latency) - 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; ((read write access) near6 latency) - 172 minimum near8 (device memory) near9 latency - 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; J	07/23 11:58 07/23 12:08
- 1405 (minimiz\$3 reduc\$3) near10 (delay near5 (access read write)) - 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; ((read write access) near6 latency) - 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO USPAT; ((read write access) near6 latency) - 172 minimum near8 (device memory) near9 latency - 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; U	07/23 11:58 07/23 12:08
- 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; US-PGPUB; EPO; JPO USPAT; (access read write))) - 44 (equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; ((read write access) near6 latency) - 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO USPAT; ((read write access) near6 latency) - 172 minimum near8 (device memory) near9 latency - 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO US-PGPUB; EPO; JP	07/23 11:58 07/23 12:08
- 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; US-PGPUB; EPO; JPO USPAT; US	07/23 12:08
- 3927 (minimiz\$3 reduc\$3) same (delay near10 (access read write)) - 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; US-PGPUB; EPO; JPO USPAT; US	07/23 12:08
- 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; (access read write))) - 44 (equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; ((read write access) near6 latency) - 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; ((read write access) near6 latency) - 172 minimum near8 (device memory) near9 latency - 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO	07/23 12:08
- 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 USPAT; US-PGPUB; EPO; JPO	
- 65 (system near5 clock) same ((minimiz\$3 reduc\$3) same (delay near10 (usPAT; us-PGPUB; EPO; JPO (read write access) near6 latency) - 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 (usPAT; us-PGPUB; EPO; JPO (uspAT; (read write access) near6 latency) - 172 minimum near8 (device memory) near9 latency - 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 (uspAT; us-PGPUB; EPO; JPO (uspAT; us-PGPUB; us-PGPUB	
(access read write))) (access read write))) (equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency) (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency) ((read write access) near6 latency) The proof of t	
- 44 (equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO US-PGPUB;)7/26 09:54
- 44 (equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 (USPAT; US-PGPUB; EPO; JPO (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 (USPAT; US-PGPUB; EPO; JPO (Iread write access) near6 latency) (ITEM (ITEM WITE access) near6 latency) (ITEM WITE access) near10 (ITEM WITE access) near6 latency)) and (ITEM WITE access) near10 (ITEM WITE access) near6 latency)) and (ITEM WITE access) near10 (ITEM WITE access) near6 latency)) and (ITEM WITE access) near10 (ITEM WITE access) near6 latency)) and (ITEM WITE access) near10 (ITEM WITE access) near6 latency)) and (ITEM WITE access) near10 (ITEM WITE access)7/26 09:54
((read write access) near6 latency) - 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO - 172 minimum near8 (device memory) near9 latency - 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO ((read write access) near6 latency)) and (minimum near8 (device us-PGPUB; memory) near9 latency) ((read write access) near6 latency)) and (minimum near8 (device us-PGPUB; memory) near9 latency)	11/20 09:34
- 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; EPO; JPO US-PGPUB; EP	
- 96 (equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 (USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)) and (minimum near8 (device US-PGPUB; memory) near9 latency)	
((read write access) near6 latency) US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)) and (minimum near8 (device us-PGPUB; memory) near9 latency) EPO; JPO US-PGPUB; EPO; JPO	7/22 12:1/
- 172 minimum near8 (device memory) near9 latency - USPAT; US-PGPUB; EPO; JPO ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; ((read write access) near6 latency)) and (minimum near8 (device memory) near9 latency) EPO; JPO USPAT; US-PGPUB; EPO; JPO	1//23 12:10
- 172 minimum near8 (device memory) near9 latency USPAT; US-PGPUB; EPO; JPO ((read write access) near6 latency)) and (minimum near8 (device memory) near9 latency) USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO EPO; JPO	
US-PGPUB; EPO; JPO ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; USPAT; ((read write access) near6 latency)) and (minimum near8 (device US-PGPUB; memory) near9 latency) EPO; JPO	.= /==
- 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)) and (minimum near8 (device memory) near9 latency) EPO; JPO USPAT; 2004/0	07/23 12:11
- 12 ((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 USPAT; US-PGPUB; memory) near9 latency) and (minimum near8 (device EPO; JPO	
((read write access) near6 latency)) and (minimum near8 (device US-PGPUB; memory) near9 latency) EPO; JPO	
memory) near9 latency) EPO; JPO)7/23 12:11
1 6658523.pn. USPAT: 2004/0	
	07/26 09:53
US-PGPUB;	
EPO; JPO	
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US-PGPUB;	
EPO; JPO	
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((read write access) near6 latency) US-PGPUB;	
EPO; JPO	
	7/26 09:55
((read write access) near6 latency)) and 365/194 US-PGPUB;	
EPO; JPO	
- 11 (equaliz\$3 leveliz\$3) near10 ((read write access) near6 latency) USPAT; 2004/0	7/26 10:35
US-PGPUB;	
EPO; JPO	
- 30 (equaliz\$3) same ((read write access) near6 latencies) USPAT; 2004/6	
US-PGPUB;	07/26 10:35
EPO; JPO	7/26 10:35
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access) near6 latencies)) US-PGPUB;	
EPO; JPO	07/26 10:35 07/26 11:26
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1	S.P.G.PUB EFG. PPO	L Number	Hits	Search Text	DB	Time stamp
10 11/105 and (minimum near4 read near10 latency) 15PO, IPO	Sept. Sept	2	0	711/105 same "2"	USPAT;	2004/08/24 11:04
10 11/105 and (minimum near4 read near10 latency)	1				US-PGPUB;	
10 711/167 and (minimum near4 read near10 latency) US-PGPUB; EPO, IPO USPAT; US-PGPUB; EPO	1				EPO; JPO	
10 711/167 and (minimum near4 read near10 latency) US-PGPUB; EPO, IPO USPAT; US-PGPUB; EPO	1	3	63	minimum near4 read near10 latency		2004/08/24 11:03
Property	11/105 and (minimum near4 read near10 latency)			·		
10	10 711/105 and (minimum near4 read near10 latency)					
10	10	4	9	711/105 and (minimum near4 read near10 latency)		2004/08/24 11:04
10 711/167 and (minimum near4 read near10 latency)	10			, , , , , , , , , , , , , , , , , , ,		
10	10					
S.	1	5	10	711/167 and (minimum near4 read near10 latency)	·	2004/08/24 11:04
11/169 and (minimum near4 read near10 latency)	FPO, IPO LSPAT; US-PGPUB; EPO, IPO LSPAT; US-PGPUB;	·		7117107 and (minimum near 11000 near 10 total 10)	1	200 1100/21 1110 1
11/169 and (minimum near4 read near10 latency)	S					
1	1	6	5	711/160 and (minimum near/ read near) (latency)		2004/08/24 11:04
1	7	° 1		7 11/109 and (minimum near read near to fatelicy)		2004/06/24 11:04
3 365/194 and (minimum near4 read near10 latency) USPAT; US-PGPUB; EPO, JPO USPAT; US-PGPUB; EPO, JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPU	2004/08/24 365/194 and (minimum near4 read near10 latency) USPAT; US-PGPUB; EPO; IPO USPAT					
US-PGPUB; EPP; PPO USPAT;	September Sept	_		711/170 1 (i-i		2004/09/24 11:04
10 365/194 and (minimum near4 read near10 latency) EPO; IPO USPAT; US-PGPUB; EPO; IPO 191 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 191 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 191 365/194 and (365/194 and (((minimum maximum) near5 (latency delay)) USPAT; US-PGPUB; EPO; IPO	Sept. Sept	′	4	/11/1/0 and (minimum near4 read near10 latency)		2004/08/24 11:04
10 365/194 and (minimum near4 read near10 latency)	10 365/194 and (minimum near4 read near10 latency) USPAT; US-PGPUB; EPO; IPO USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; U	•				
1 1 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 2004/08/24 1 US-PGPUB; EPO; IPO USPAT; US-PG	9 91 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 10 53 711/169 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 11 91 365/194 and (365/194 and (((minimum maximum) near5 (latency delay))) and (memory near5 (module banks))) 11 91 365/194 and (365/194 and ((((minimum maximum) near5 (latency delay))) and (memory near5 (module banks))) 11 91 365/194 and (365/194 and ((((minimum maximum) near5 (latency delay))) us.PoPOJUB; EPO; JPO USPAT; US-POPUB; EPO; JPO USPAT; USPAT			255/104 17 17 17 17 17 17 17 17 17 17 17 17 17		0004/00/2: : : :
1 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 2004/08/24 1 US-PGPUB; EPO; IPO USPAT; US-PGPUB;	9 9 1 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 10 53 711/169 and ((((minimum maximum) near5 (latency delay))) and (memory near5 (module banks))) 11 91 365/194 and (365/194 and ((((minimum maximum) near5 (latency delay))) and (memory near5 (module banks)))) 12 91 365/194 and (365/194 and (((((minimum maximum) near5 (latency delay))) uSPAT; US-PGPUB; EPO; JPO	8	10	365/194 and (minimum near4 read near10 latency)		2004/08/24 11:04
1 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks)))	9 91 365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 10 53 711/169 and ((((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 11 91 365/194 and (365/194 and ((((minimum maximum) near5 (latency delay)) und (memory near5 (module banks)))) 2004/08/24 11 91 365/194 and (365/194 and ((((minimum maximum) near5 (latency delay)) und (memory near5 (module banks)))) 2004/08/24 12 2004/08/24					
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10 53 711/169 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 2004/08/24 l USPAT; US-PGPUB; EPO; JPO USPAT	10 53 711/169 and ((((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))) 2004/08/24 USPAT; USPGPUB; EPO; IPO USP	9	91		,	2004/08/24 11:05
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near5 (module banks)))						
1 91 365/194 and (365/194 and ((((minimum maximum) near5 (latency delay)) 1 1 1 1 1 1 1 1 1	Proper Property Pr	10	53	711/169 and (((minimum maximum) near5 (latency delay)) and (memory	USPAT;	2004/08/24 11:05
1 365/194 and (365/194 and (((((minimum maximum) near5 (latency delay))) and (((memory near5 (module banks)))) and (((memory near5 (module banks))))	11			near5 (module banks)))	US-PGPUB;	
September Sept	and (memory near5 (module banks)))) - 756 (system cpu) near10 (read near5 (latency delay)) - 965 (system cpu) near10 (read near5 (latency delay)) - 965 (system cpu) near10 (read near6 (latency delay)) - 965 (system cpu) near10 (read near6 (latency delay))) same (device near10 (system cpu) near10 (read near5 (latency delay))) same (device near10 (system cpu) near10 (read near4 latency) - 8 sum near10 (device near4 read near4 latency) - 8 sum near10 (device near4 read near4 latency) - 10 ((system cpu) near10 (read near5 (latency delay))) and (sum near10 (system cpu) near10 (read near5 (latency delay))) and (sum near10 (system cpu) near10 (read near6 (latency delay))) same (sum near10 (system cpu) near10 (read near6 (latency delay))) same (sum near10 (system cpu) near10 (device near4 read near4 latency) - 11 (sum\$3 add\$3) near10 (device near4 read near4 latency) - 24 (device near10 (read near5 (latency delay))) near10 maximum - 25 (minimum near5 read near3 (latency delay))) near10 maximum - 15 (minimum near5 read near3 (latency delay))) and (memory near5 (module banks)) - 1570 ((minimum maximum) near5 (latency delay))) and (memory near5 (sp. jp0				EPO; JPO	
September Sept	and (memory near5 (module banks)))) - 756 (system cpu) near10 (read near5 (latency delay)) - 965 (system cpu) near10 (read near5 (latency delay)) - 965 (system cpu) near10 (read near6 (latency delay)) - 966 (system cpu) near10 (read near6 (latency delay))) same (device near10 - 67 ((system cpu) near10 (read near5 (latency delay))) same (device near10 - 7 ((system cpu) near10 (read near4 latency) - 8 sum near10 (device near4 read near4 latency) - 8 sum near10 (device near4 read near4 latency) - 7 ((system cpu) near10 (read near5 (latency delay))) and (sum near10 - 7 ((system cpu) near10 (read near5 (latency delay))) same (sum near10 - 7 ((system cpu) near10 (read near5 (latency delay))) same (sum near10 - 7 ((system cpu) near10 (read near4 read near4 latency) - 7 ((system cpu) near10 (device near4 read near4 latency) - 7 ((system cpu) near10 (read near5 (latency delay))) same (sum near10 - 10 (sum\$3 add\$3) near10 (device near4 read near4 latency) - 2004/07/15 - 24 (device near10 (read near5 (latency delay))) near10 maximum - 2004/07/15 - 24 (device near10 (read near6 (latency delay))) near10 maximum - 55 (minimum near5 read near3 (latency delay))) and (memory near5 (module banks)) - 1570 ((minimum maximum) near5 (latency delay))) and (memory near5 (module banks)) - 1570 ((minimum maximum) near5 (latency delay))) and (memory near5 (module banks))	11	91	365/194 and (365/194 and (((minimum maximum) near5 (latency delay))		2004/08/24 11:05
EPC; IPO USPAT; US-PGPUB; EPO; IPO USPAT; US-PGPUB;	- 756 (system cpu) near10 (read near5 (latency delay)) - 965 device near10 (read near7 (latency delay)) - 965 device near10 (read near7 (latency delay)) - 67 ((system cpu) near10 (read near5 (latency delay))) same (device near10 (read near7 (latency delay))) - 8 sum near10 (device near4 read near4 latency) - 8 sum near10 (device near4 read near4 latency) - 17 ((system cpu) near10 (read near5 (latency delay))) and (sum near10 (device near4 read near4 latenc\$3) - 7 ((system cpu) near10 (read near5 (latency delay))) same (sum near10 (device near4 read near4 latenc\$3)) - 7 ((system cpu) near10 (read near5 (latency delay))) same (sum near10 (device near4 read near4 latenc\$3)) - 18 (sum\$3 add\$3) near10 (device near4 read near4 latency) - 2004/07/15 - 24 (device near4 read near4 (latency delay))) near10 maximum - 24 (device near10 (read near5 (latency delay))) near10 maximum - 25 (minimum near5 read near3 (latency delay))) and (memory near5 (module banks)) - 1570 ((minimum maximum) near5 (latency delay))) and (memory near5 (module banks)) - 1570 ((minimum maximum) near5 (latency delay))) and (memory near5 (module banks)) - 1570 ((minimum maximum) near5 (latency delay))) and (memory near5 (module banks))					
156 (system cpu) near10 (read near5 (latency delay)) USPAT; US-PGPUB; EPO; IPO	- 756 (system cpu) near10 (read near5 (latency delay)) - 965 device near10 (read near7 (latency delay)) - 67 ((system cpu) near10 (read near5 (latency delay))) same (device near10 USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; E					
US-PGPUB; EPO; JPO USPAT;	US-PGPUB; EPO; IPO USPAT; US-PGPUB; EPO; IPO	_	756	(system cnu) near10 (read near5 (latency delay))		2004/07/15 15:47
Series S	- 965 device near10 (read near7 (latency delay)) - 67 ((system cpu) near10 (read near5 (latency delay))) same (device near10 USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO;			(cycloin opu) nom to (tout nom) (tutono) tou)))		200 0
965 device near10 (read near7 (latency delay))	- 965 device near10 (read near7 (latency delay)) - 67 ((system cpu) near10 (read near5 (latency delay))) same (device near10 USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO;					
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67 ((system cpu) near10 (read near5 (latency delay))) same (device near10 (USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO;	FPO; JPO			device nearly (read near (latency delay))		2001/07/13 13:51
((system cpu) near10 (read near5 (latency delay))) same (device near10 (read near7 (latency delay))) 8 sum near10 (device near4 read near4 latency) 8 sum near10 (device near4 read near4 latencs) 10	- ((system cpu) near10 (read near5 (latency delay))) same (device near10 (USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO;			•		
(read near7 (latency delay))) US-PGPUB; EPO; IPO USPAT; US-PGPUB; US-PGPUB; US-PGPUB; US-PGPUB; US-PGPUB; US-PGPUB; US-PGPUB; US-PGPUB	Cread near7 (latency delay)))	_	67	((system cnu) near10 (read near5 (latency delay))) same (device near10		2004/07/15 15:23
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8 sum near10 (device near4 read near4 latenc\$3) 7 ((system cpu) near10 (read near5 (latency delay))) and (sum near10 (device near4 read near4 latenc\$3)) 7 ((system cpu) near10 (read near5 (latency delay))) same (sum near10 (device near4 read near4 latenc\$3)) 11 (sum\$3 add\$3) near10 (device near4 read near4 latency) 12 (device near10 (read near5 (latency delay))) near10 maximum 13 (device near10 (read near6 (latency delay))) near10 maximum 14 (device near10 (read near7 (latency delay))) near10 maximum 15 (minimum near5 read near3 (latency delay)) and (memory near5 (module banks)) 15 ((minimum maximum) near5 (latency delay)) and (memory near5 (module banks)) 15 ((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))	sum near10 (device near4 read near4 latenc\$3) ((system cpu) near10 (read near5 (latency delay))) and (sum near10 USPAT; US-PGPUB; EPO; JPO USPAT; (device near4 read near4 latenc\$3)) ((system cpu) near10 (read near5 (latency delay))) same (sum near10 USPAT; US-PGPUB; EPO; JPO USPAT; (device near4 read near4 latenc\$3)) ((sum\$3 add\$3) near10 (device near4 read near4 latency) ((sum\$3 add\$3) near10 (device near4 read near4 latency) ((device near10 (read near7 (latency delay))) near10 maximum (device near10 (read near5 (latency delay))) near10 maximum (uspat; Us-PGPUB; EPO; JPO USPAT; Us-PGPUB; EPO; JPO US		·			
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7 ((system cpu) near10 (read near5 (latency delay))) same (sum near10 (USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JP	- ((system cpu) near10 (read near5 (latency delay))) same (sum near10 (USPAT; US-PGPUB; EPO; JPO (sum\$3 add\$3) near10 (device near4 read near4 latency) USPAT; US-PGPUB; EPO; JPO (device near10 (read near7 (latency delay))) near10 maximum USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO (minimum near5 read near3 (latency delay)) and (memory near5 (module banks)) USPAT; US-PGPUB; EPO; JPO (minimum maximum) near5 (latency delay)) and (memory near5 (module banks)) USPAT; USPGPUB; EPO; JPO USPAT; USPGPUB; EPO; JPO USPAT; USPAT; USPGPUB; EPO; JPO USPAT; USPAT			(device near4 read near4 latenc\$3))		
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US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; EPO; EPO; EPO; EPO; EPO; EPO;	- S5 (minimum near5 read near3 (latency delay)) and (memory near5 (module banks)) - US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; USPAT; 2004/07/15		24	(device near10 (read near7 (latency delay))) near10 maximum		2004/07/15 15:32
(minimum near5 read near3 (latency delay)) and (memory near5 (module banks)) (minimum near5 read near3 (latency delay)) and (memory near5 (module banks)) ((minimum maximum) near5 (latency delay)) and (memory near5 USPAT; 2004/07/15 1	- S5 (minimum near5 read near3 (latency delay)) and (memory near5 (module banks)) - USPAT; US-PGPUB; EPO; JPO ((minimum maximum) near5 (latency delay)) and (memory near5 USPAT; 2004/07/15	- 1		(,, , , , , , , , , , , , ,		
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1570 ((minimum maximum) near5 (latency delay)) and (memory near5 EPO; JPO USPAT; 2004/07/15 1	EPO; JPO USPAT; 2004/07/15		55			2007/0//13 13:4/
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		-	55	banks))		
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	EPO; JPO	-		((minimum maximum) near5 (latency delay)) and (memory near5	EPO; JPO USPAT;	2004/07/15 15:48
[[(modula honka))	(Infoquie panks)) UN-PGPUR'		22			2004/(